

Patent

Docket No.: Intel 2207/979602

Assignee: Intel Corporation

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANTS : Ronny RONEN et al.

SERIAL NO. OF  
PARENT APPLICATION : 09/752,233

FILING DATE OF  
PARENT APPLICATION : December 29, 2000

FOR : SYSTEM AND METHOD FOR FUSING  
INSTRUCTIONS

ART UNIT OF  
PARENT APPLICATION : 2122

EXAMINER OF  
PARENT APPLICATION : Chameli DAS

M/S: PATENT APPLICATION  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Certificate of Mailing	
I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail No. EV351181058US in an envelope addressed to: M/S: PATENT APPLICATION, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on	
Date: January 6, 2004	Signature: <u>Barbara Vance</u> Barbara Vance

**INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

Submitted herewith is an Information Disclosure Statement under 37 CFR §1.97(b)(3) with twelve (12) reference(s) listed on the attached PTO-1449 (modified) form. A copy is not enclosed since the present application was filed after June 30, 2003. (See OG Dated: August 5, 2003).

It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear

among the "References Cited" on any patent to issue therefrom.

If any fee is required, the Office is hereby authorized to charge any fees, or credit any overpayments under 37 CFR §1.17(p) to Kenyon & Kenyon, Deposit Account No. 11-0600.

Respectfully submitted,

KENYON & KENYON

Dated: January 6, 2004

By: Stephen T. Neal  
Stephen T. Neal  
(Reg. No. 47,815)  
Attorneys for Intel Corporation

KENYON & KENYON  
333 West San Carlos St., Suite 600  
San Jose, CA 95110

Telephone: (408) 975-7500  
Facsimile: (408) 975-7501

<b>Form PTO-1449 (modified)</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT</b>	<b>Attorney Docket No.</b> Intel 2207/979602	<b>Serial No.</b> 09/752,233 (Parent)
	<b>Applicant</b> Ronny RONEN et al.	
	<b>Filing Date</b> December 29, 2000 (Parent)	<b>Group Art Unit</b> 2122 (Parent)

**U. S. PATENT DOCUMENTS**

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
/C.K./	**5,392,228	February 21, 1995	Burgess et al.	364	715.04	December 6, 1993
/C.K./	**5,903,761	May 11, 1999	Tyma	395	709	October 31, 1997
/C.K./	**5,957,997	September 28, 1999	Olson et al.	708	205	April 25, 1997
/C.K./	**6,006,324	December 21, 1999	Tran et al.	712	204	October 29, 1998
/C.K./	**6,018,799	January 25, 2000	Wallace et al.	712	300	July 22, 1998
/C.K./	**6,151,618	November 21, 2000	Wahbe et al.	709	1	June 18, 1997
/C.K./	**6,247,113 B1	June 12, 2001	Jaggar	712	200	May 27, 1998
/C.K./	**6,282,634 B1	August 28, 2001	Hinds et al.	712	210	May 27, 1998

\*\*A copy is not enclosed since the present application was filed after June 30, 2003. (See OG Dated: August 5, 2003)

**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

**OTHER DOCUMENTS**

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/C.K./	Perng-Yi Ma, TRW Systems Group and T.G. Lewis, Oregon State University, "Design of a Machine-Independent Optimizing System for Emulator Development," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 2, No. 2, April 1980, pps. 239-262.
/C.K./	G. J. Lipovski and Paul Vaughan, Department of Electrical and Computer Engineering, University of Texas, Austin, Texas, "A Fetch-And-Op Implementation for Parallel Computers," <i>CH2545-2/88/0000/0384\$01.00 © 1988 IEEE</i> , pps. 384-392
/C.K./	Guy Argo, Computing Science Department, The University, Glasgow G12 8QQ, United Kingdom, "Improving the Three Instruction Machine," © 1989 <i>ACM 0-89791-328-0/89/0009/0100 \$1.50</i> , pps.100-115
/C.K./	Soo-Mook Moon and Kemal Ebcioglu, IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598, "An Efficient Resource-Constrained Global Scheduling Technique for Superscalar and VLIW processors," <i>0-8186-3175-9/92 \$3.00 © 1992 IEEE</i> , pps. 55-71

\*\*A copy is not enclosed since the present application was filed after June 30, 2003. (See OG Dated: August 5, 2003)

EXAMINER	/Chuck Kendall/	DATE CONSIDERED	06/08/2008
<p>EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>			